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A Review On Various Multilevel Inverter Topologies

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ABSTRACT
Multi-level inverters play a key role in today's microgrids with renewable energy sources. It is a power electronic device that is used for high voltage and high power applications, with the added advantages of low switching stress and lower total harmonic distortion (THD), hence reducing the size and bulk of the passive filters. It gives the output current waveform which is nearly sinusoidal in nature. This paper presents a review on various types of multilevel inverter. Therefore with less number of switches in the circuit, there will be reduction in the gate driver circuits, weight and reduces the THD . A five level inverter will be simulated with the implementation of PWM techniques and its effect on the harmonic spectrum will be analyzed. The system will be modelled with the help of MATLAB/SIMULINK. (This paper compares different topologies of inverters (Diode clamped inverter, Flying capacitor clamped inverter, Cascaded H-bridge inverter and asymmetrical MLI).

Keywords
Multilevel inverter, PWM, CMLI, DMLI, FCMLI.

1. INTRODUCTION
Multi Level Inverter (MLI) is a power electronic system that produces output voltage from several levels of DC input voltages. The attractive feature of this technology is mainly in the range of medium to high voltage application and offers a number of advantages when compared to the conventional two-level inverter. Multilevel inverters are used in power conversion system due to improved voltage and current waveforms. It is recently emerged as very important alternatives in high power medium voltage applications because of their advantage over the conventional one and their capability to reduce the undesirable harmonics. So that performance and efficiency of the system is improved. The concept of multilevel inverter is introduced with an aim to reduce switching losses and to obtain the output voltage with multiple steps to achieve the improved power quality and higher voltage capability. Multilevel inverters are used in high voltage AC motor drive, distributive generation, high voltage direct transmission as well as SVC applications. Pharne and Bhosale [1] made a review on multilevel inverter topology. Prasad et al [2] discussed different topologies of CMLI. Lakshmi et al [3] discussed cascaded seven level inverter with reduced number of switches using level shifting PWM technique. Najafi et al [4] evaluated a new design of a multilevel inverter topology. Ebrahimi et al [5] introduced a new multilevel converter topology with reduced number. Roshankumar et al [6] deals a five-level inverter topology with single-DC supply by cascading a flying capacitor inverter. Jacob et al [7] suggested a multilevel inverter with reduced number of switches. Rahilal et al [8] evaluated a new 81 level inverter with reduced number of switches. Babaei in [9] proposed a new cascaded multilevel inverter with reduced number of switches. James et al [10] proposed a multilevel inverter with reduced number of switches. Sun et al [11] deals on multi-level Inverter capable of power factor control.

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Adam et al [12] decribes a quasi-two-level and three-level operation of a diode-clamped multilevel inverter using space vector modulation. Gupta et al [13] made a topology for multilevel inverters to attain maximum number of levels from given DC sources. Lakshmi and Chandra [14] made a comparison of symmetrical and asymmetrical multilevel inverters. Ebrahimi et al [15] suggested a new topology of cascaded multilevel converters with reduced number of components for high voltage applications. Caballero et al [16] made on symmetrical hybrid multilevel inverter concept based on multi-state switching cells. Suroso et al [17] describe a multilevel voltage-source inverter two-level power modules. Rahim et al [18] proposed a transistor-clamped H-bridge based with new method of capacitor voltage balancing. Murugesan et al [19] proposed a new multilevel inverter topology using less number of switches. Dixon et al [20] discussed on asymmetrical multilevel inverter for traction drives using one DC supply. Rokan [21] discussed new multilevel inverter topology with reduced switch count. [22] & [24] made a new multilevel inverter topology with reduced number of switches. Arif et al [23] proposed a modified cascaded multilevel inverter with reduced switch count employing bypass diodes. Lezana et al [25] made a class of cascaded multilevel inverter with regeneration capability and reduced number of switches. Daher et al [26] described a multilevel inverter topologies for stand-alone PV systems. Tehrani etal [27] deals novel multilevel inverter. Panagis [28] made a comparison of state of the art multilevel inverters. Chen et al [29] analysis novel multilevel inverter topology with no clamping diodes and flying capacitors. Zhang et al [30] made a novel modulation technology for multilevel inverter based on equivalent area. Chaturvedi et al [31] made a investigations on different multilevel inverter control techniques by simulation. Zhong et al [32] discussed a cascade multilevel inverter using a single DC source. Ceglia et al [33] proposed a new multilevel inverter topology. Sung-yong et al [34] describes a novel hybrid multilevel inverter using DC-link voltage combination. Rodriguez et al [35] carried out a survey of multilevel inverter topologies, controls and applications. Soto et al [36] proposed a comparison of high power converter topologies for the implementation of FACTS controllers. Dong kim et al [37] made a generalized under land snubber for flying capacitor multilevel inverter and converter. Ryan et al [38] introduces a control topology for single-phase UPS inverter.

2. TYPES OF MULTILEVEL INVERTER

Nowadays, multilevel inverters are widely used in power industry. It starts from three level inverter. Voltage unbalance problem is one of the major issue in working of multilevel inverter. The multilevel inverters are classified as follows:

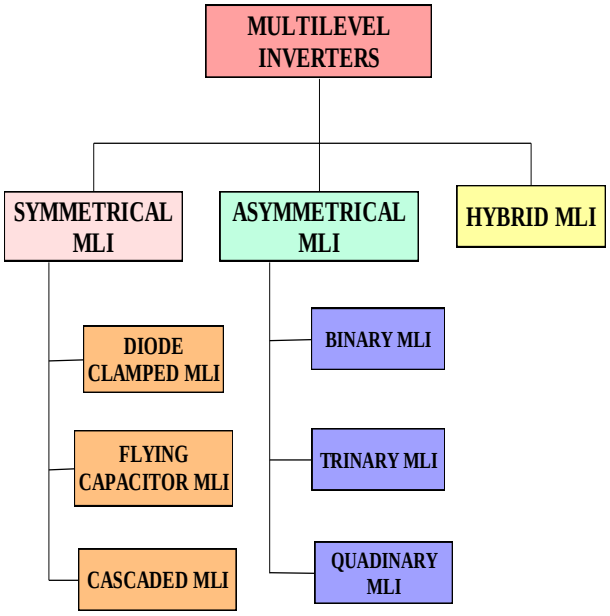

Fig 1: Types of multilevel Inverters

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3. MULTILEVEL INVERTER TOPOLOGIES

The multilevel inverter topology is broadly classified as symmetrical (with equal source voltages), asymmetrical (with unequal source voltages) and hybrid inverters.

3.1 Symmetrical Multilevel Inverters

Symmetrical multilevel inverter is defined as inverter with equal amplitude of voltage sources. For example, if 100V of DC sources is used for one source than all sources have 100V.

3.1.1 Diode clamped multilevel inverter

The main concept of this inverter is to use diodes to limit the power devices voltage stress. The voltage over each capacitor and each switch is V_{dc}. An *m* level inverter needs (*m*-1) voltage sources, (m-1) capacitors, 2(*m*-1) switching devices and (*m*-1) (*m*-2) diodes per leg.

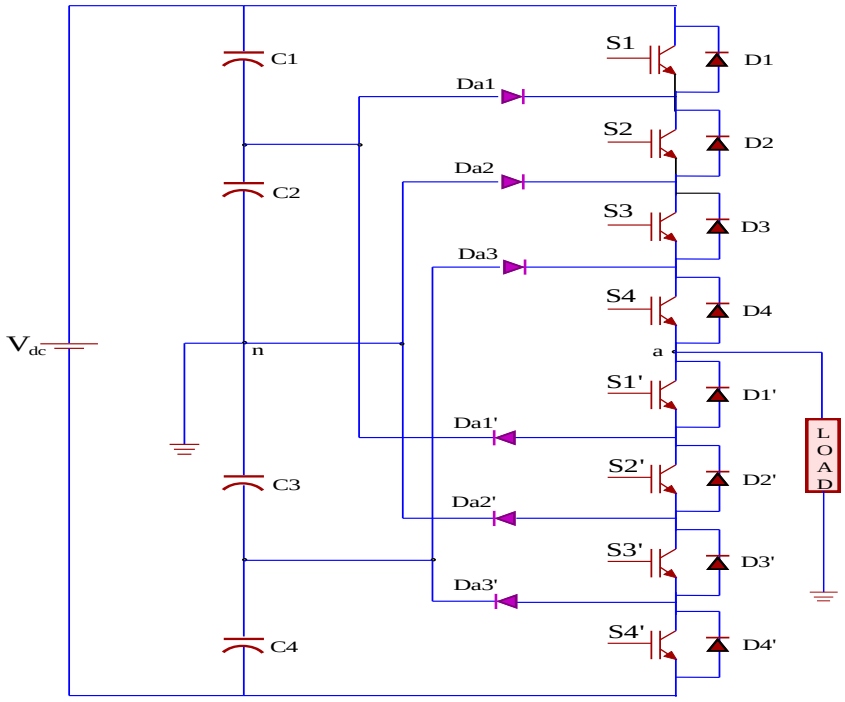

Fig 2: Five level diode clamped multilevel inverter

Table 1: Diode clamped inverter - switch states and output voltage levels

Switch state								Output
S1	**S2**	**S3**	**S4**	**S1'**	**S2'**	**S3'**	**S4'**	**V_{an}**
1	1	1	1	0	0	0	0	$+V_{dc}/2$
0	1	1	1	1	0	0	0	$+V_{dc}/4$
0	0	1	1	1	1	0	0	0
0	0	0	1	1	1	1	0	$-V_{dc}/4$
0	0	0	0	1	1	1	1	$-V_{dc}/2$

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3.1.1.1 ***Principal of operation***

To produce a staircase-output voltage, let us consider only one leg of the five –level inverter, as shown in figure 2, as an example. A single –phase bridge with two legs is shown in figure 3. The dc rail 0 is the reference point of the output phase voltage. The steps to synthesize the five level voltages are as follows:

1. For an output voltage level $v_{a0} = V_{dc}$, turn on all upper-half switches Sa1 through S_{a4}.
2. For an output voltage level $v_{a0} = V_{dc}/2$, turn on two upper switches S_{a3} through S_{a4} and two lower switches S'_{a1} and S'_{a2}.
3. For an output voltage level $v_{a0} = 0$, turn on all lower half switches S'_{a1} through S'_{a4}.

State condition 1 means the switch is on, and state 0 means the switch is off. It should be noticed that each switch is turned on only once per cycle and there are four complementary switch pairs in each phase. These pairs for one leg of the inverter are (S_{a1}, S'_{a1}), (S_{a2}, S'_{a2}), (S_{a3}, S'_{a3}) and (S_{a4}, S'_{a4}). Thus, if one of the complementary switch pairs is turned on, the other of the same pair must be off. Four switches are always turns on at the same time. The line voltage consists of the positive phase- leg voltage of terminal *a* and the negative phase-leg voltage of terminal *b*. Each phase-leg voltage tracks one-half of the sinusoidal wave. The resulting line voltage is a five-level staircase wave. This implies that an *m*-level converter has an *m*-level output phase-leg voltage and a (2*m*-1) level output line voltage.

The switching angles should be calculated in such a way that the THD of the output voltage becomes as low as possible. The switching angle calculation method that is used in this thesis is the harmonic elimination method. In this method the lower dominant harmonics can be eliminated by choosing calculated switching angles.

3.1.1.2 Features

1. High-voltage rating required for blocking diodes.
2. Unequal device rating.
3. Capacitor voltage unbalance.

3.1.1.3 Advantages

1. High efficiency.
2. No need of filters to reduce harmonics.
3. Reactive power flow can be controlled.
4. Control method is simple.

3.1.1.4 Disadvantages

1. For high levels, more number of diodes are required.
2. Real power flow control for individual converter is difficult.

3.1.2 Flying capacitor multilevel inverter

This inverter uses capacitors to limit the voltage of the power devices. The configuration of the flying capacitor multilevel inverter is like a diode clamped multilevel inverter except that capacitors are used to divide the input DC voltage. The voltage over each capacitor and each switch is *Vdc*. Figure 3 shows the flying capacitors based multilevel inverter topology. It requires (m-1) capacitors on dc bus form level converter.

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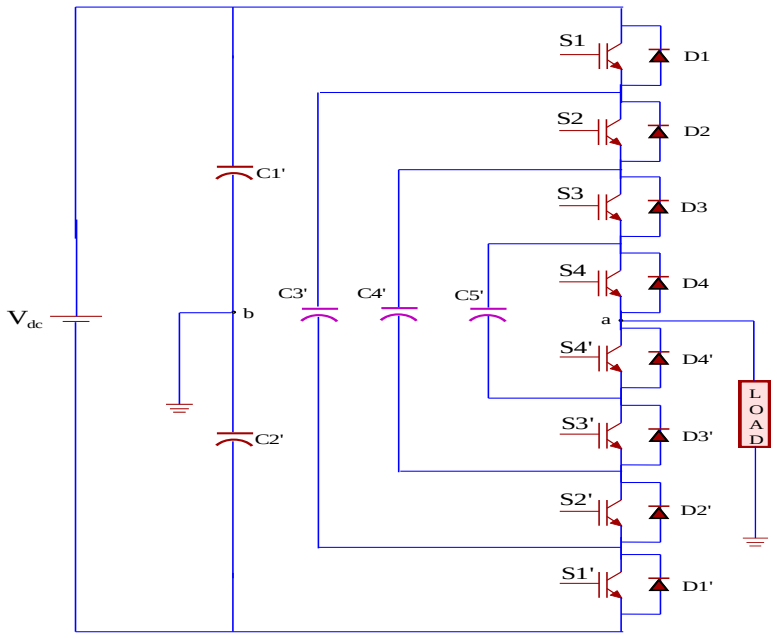

Fig 3: Five level flying capacitor based multilevel inverter.

Table 2: Flying capacitor inverter-switch states and output voltage levels

S1	S2	S3	S4	C3'	C4'	C5'	V_{ab}
1	1	1	1	NC	NC	NC	$+V_{dc}/2$
1	1	1	0	NC	NC	+	$+V_{dc}/4$
1	1	0	1	NC	+	-	
1	0	1	1	+	-	NC	
0	1	1	1	-	NC	NC	
0	0	1	1	NC	-	NC	0
0	1	0	1	-	+	-	
0	1	1	0	-	NC	+	
1	0	0	1	+	NC	-	
1	0	1	0	+	-	+	
1	1	0	0	NC	+	NC	
1	0	0	0	+	NC	NC	$-V_{dc}/4$
0	1	0	0	-	+	NC	
0	0	1	0	NC	-	+	
0	0	0	1	NC	NC	-	
0	0	0	0	NC	NC	NC	$-V_{dc}/2$

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3.1.2.1 Features

1. Large number of capacitors.
2. Balancing capacitor voltages.

3.1.2.2 Advantages

1. Extra ride through capability during power outage.
2. No need of filters to reduce harmonics.
3. It gives proper switching combination to balance different voltage levels.
4. Real and reactive power flow can be controlled.

3.1.2.3 Disadvantages

1. High numbers of capacitors are required for high level.
2. For real power transmission switching frequency and losses are high.

3.1.3 Cascaded multilevel inverter

The concept of this inverter is based on connecting H-bridge inverters in series to get a sinusoidal voltage output. The output voltage is the sum of the voltage that is generated by each cell. The number of output voltage levels are $2n+1$, where n is the number of cells. The switching angles can be chosen in such a way that the total harmonic distortion is minimized. One of the advantages of this type of multilevel inverter is that it needs less number of components comparative to the Diode clamped or the flying capacitor, so the price and the weight of the inverter is less than that of the two former types.

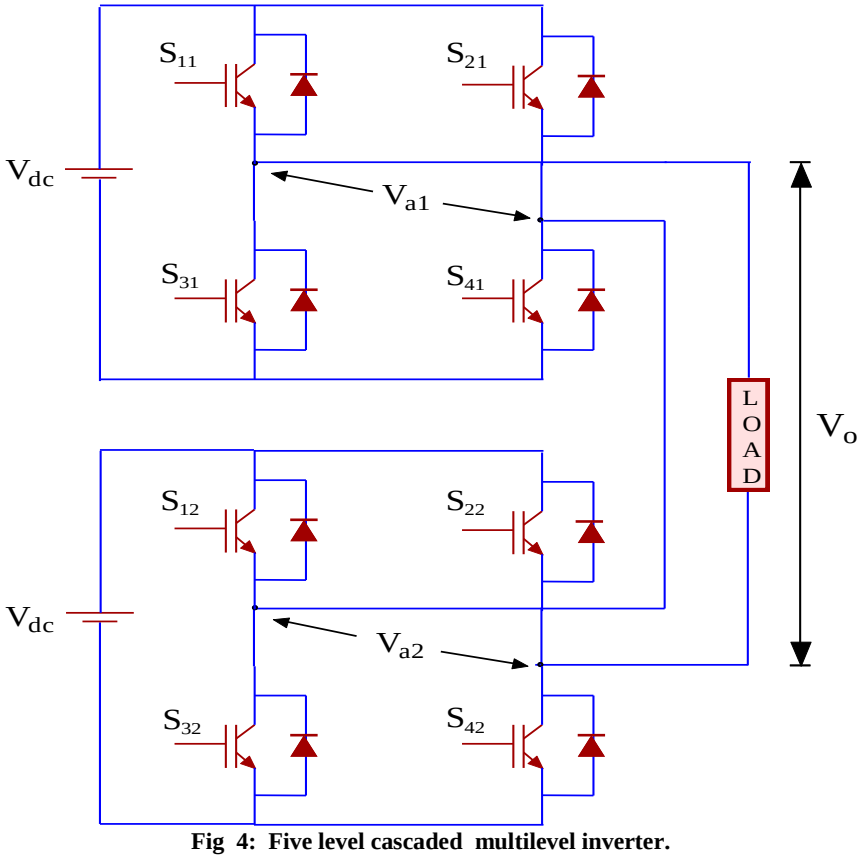

Fig 4: Five level cascaded multilevel inverter.

Fig. 4 shows an five level cascaded H-bridge multilevel inverter. The switching angles calculation method that is used in this inverter is the same as for the previous multilevel inverters. An m level cascaded H-bridge multilevel inverter needs $2(m-1)$ switching devices where m is the number of the output voltage level. This inverter can maintain a strategic distance from additional bracing diodes or voltage adjusting capacitors.

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Table 3: Switch states and voltage levels of five level cascaded inverter

S_{11}	S_{21}	S_{12}	S_{22}	Output (V_o)
1	0	1	0	$+2V_{dc}$
1	0	0	0	$+V_{dc}$
1	0	1	1	$+V_{dc}$
0	0	1	0	$+V_{dc}$
1	1	1	0	$+V_{dc}$
0	0	0	0	0
1	1	1	1	0
1	0	0	1	0
0	1	1	0	0
0	0	1	1	0
1	1	0	0	0
0	1	1	1	$-V_{dc}$
0	1	0	0	$-V_{dc}$
1	1	0	1	$-V_{dc}$
0	0	0	1	$-V_{dc}$
0	1	0	1	$-2V_{dc}$

3.1.3.1 ***Features***

1. Separate dc source are fuel cell, photovoltaic, and biomass.
2. Back-to-back fashion between two converter is not possible.

3.1.3.2 ***Advantages***

1. Less number of components is needed for getting same number of voltage level.
2. No need of extra diodes and capacitors
3. Because of same structure it allows the scalable, modularized circuit layout and packaging.

3.1.3.3 Disadvantages

1. Separate DC sources are required for the real power conversion.

The figure below shows the simulated model using eight Ideal switches. In a practical scenario each of the switches requires a separate gate driver circuit. DC power source of 100 Volts are used and a load of 10 ohms. Before implementing the Multicarrier PWM Techniques, simulations were conducted by comparing a triangular wave and a constant value at specific intervals of time producing the characteristic multistep output waveform. Based on the PWM techniques, the harmonic spectrum was analysed using the FFT Window in MATLAB/Simulink.

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3.2 Asymmetrical Multilevel Inverters

3.2.1 Binary multilevel inverter

Fig. 5 shows a circuit configuration of a cascaded H-bridge multilevel inverter employing binary dc input source. It looks like a traditional cascaded H-bridge multilevel inverter except input dc sources. By using Vdc and 2Vdc, it can synthesize five output levels; -2Vdc, -Vdc, 0, Vdc, 2Vdc.The lower inverter generates a fundamental output voltage with two levels, and then the upper inverter adds or subtracts one level from the fundamental wave to synthesize stepped waves. Here, the final output voltage levels becomes the sum of each terminal voltage of H-bridge, and it is given as

$$\mathbf{V}_{out} = V_{HB1} + V_{HB2} \qquad (1)$$

In the proposed circuit topology, if *n* number of H-bridge module has independent DC sources in sequence of the power of 2, an expected output voltage level is given as

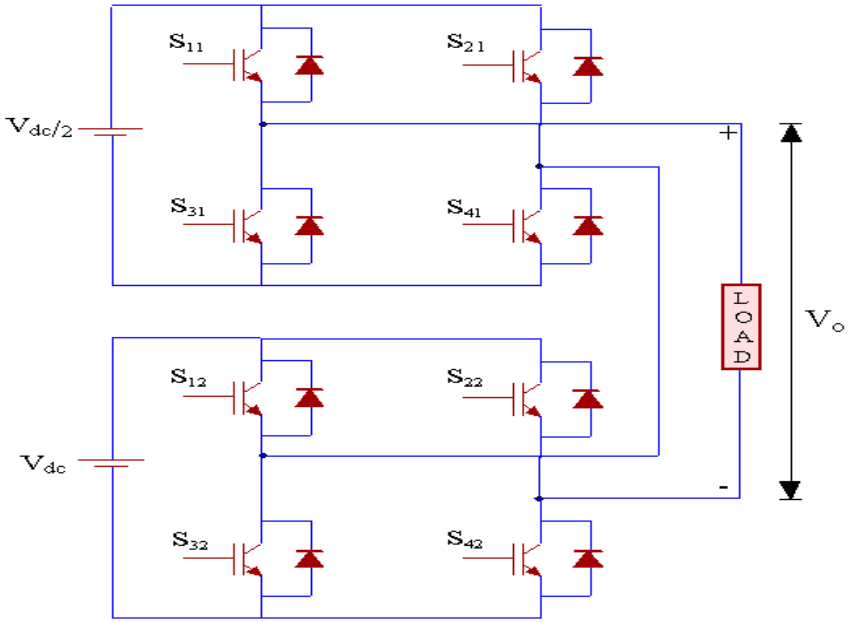

Fig. 5: Binary DC source MLI

3.2.2 Trinary multilevel inverter

Fig. 6 shows a circuit configuration of a cascaded H-bridge multilevel inverter employing trinary dc input source. It looks like a traditional cascaded H-bridge multilevel inverter except input dc sources. By using Vdc and 3Vdc, it can synthesize five output levels; -3Vdc, -Vdc, 0, Vdc, 3Vdc. The lower inverter generates a fundamental output voltage with three levels, and then the upper inverter adds or subtracts one level from the fundamental wave to synthesize stepped waves. Here, the final output voltage levels becomes the sum of each terminal voltage of H-bridge, and it is given as

$$\mathbf{V}_{out} = V_{HB1} + V_{HB2} \qquad (3)$$

In the proposed circuit topology, if *n* number of H-bridge module has independent DC sources in sequence of the power of 3, an expected output voltage level is given as

$$V_n = 3^n,\ n = 1,2,3.. \qquad (4)$$

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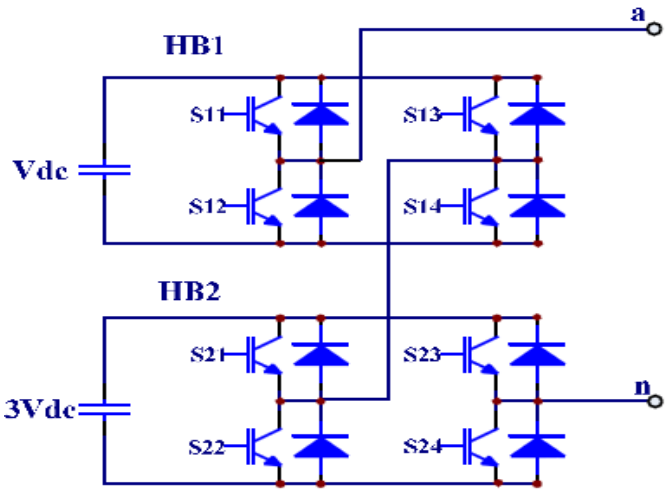

Fig. 6: Trinary DC source MLI

Based on the PWM techniques, the harmonic spectrum was analysed using the FFT Window in MATLAB/Simulink.

3.2.3 Quadinary multilevel inverter

Fig. 7 shows a circuit configuration of a cascaded H-bridge multilevel inverter employing quadinary dc input source. It looks like a traditional cascaded H-bridge multilevel inverter except input dc sources. By using Vdc and 4Vdc, it can synthesize five output levels;-4Vdc, -Vdc, 0, Vdc, 4Vdc.

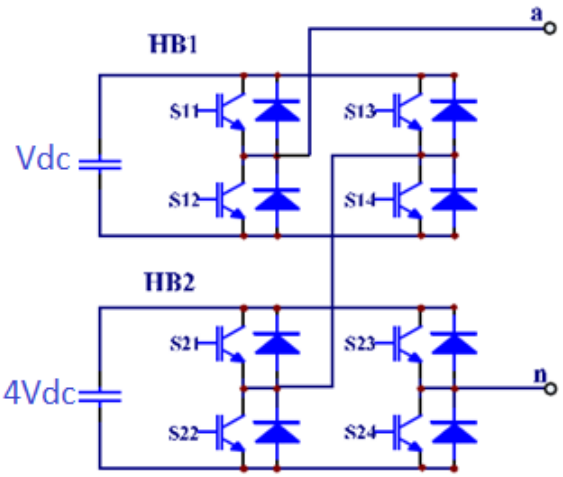

Fig. 7: Quadinary DC source MLI

The lower inverter generates a fundamental output voltage with four levels, and then the upper inverter adds or subtracts one level from the fundamental wave to synthesize stepped waves. Here, the final output voltage levels becomes the sum of each terminal voltage of H-bridge and it is given as

$$\mathbf{V}_{out} = V_{HB1} + V_{HB2} \qquad (5)$$

In the proposed circuit topology, if *n* number of H-bridge module has independent DC sources in sequence of the power of 4, an expected output voltage level is given as

$$V_n = 4^n,\ n = 1,2,3.. \qquad (6)$$

Table 4. Comparison of components required for various topologies

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S. No.	DCMLI (5-level)	FCMLI (5-level)	CMLI (5-level)	Binary MLI (7-level)	Trinary MLI (9-level)	Quadinary MLI (11-level)
Main switching devices	8	8	8	8	8	8
Clamping diodes	12	0	0	0	0	0
Balancing capacitors	0	12	0	0	0	0
DC bus capacitors	4	4	2	2	2	2
Main diodes	8	8	8	8	8	8

4. CONCLUSIONS

In this paper various types of multilevel inverter topologies are discussed and compared. Cascaded multilevel inverter requires minimum number of components when compared will other types (it is shown in Table.4). So it produce an increased stepped output with less number of semiconductor switches. With fewer switches, controlling the overall circuit becomes less complex, the size and installation area reduces. Whenever the demand increases it is met out by adding additional H-bridge in cascaded inverter. Also the various new topologies for cascaded inverter are available to decreases the switching devices. Based on the simulation results the Multicarrier PWM techniques produced a lower THD than with PWM technique involving the comparison between triangular and constant values. An amplitude modulation index less than unity did decrease the overall THD though the high presence of lower order harmonics made it an unsuitable choice to use it with a filter design. In conclusion an amplitude modulation equal or less than one would produce a desirable output.

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